Ultra-Thin Phase-Change Bridge Memory Device Using GeSb

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IBM/Qimonda/Macronix PCRAM Joint Project

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Abstract

An ultra-thin phase-change bridge (PCB) memory cell, implemented with doped GeSb, is shown with $<100\mu$A RESET current. The device concept provides for simplified scaling to small cross-sectional area (60nm^2) through ultra-thin (3nm) films; the doped GeSb phase-change material offers the potential for both fast crystallization and good data retention.

Introduction

Phase-Change Memory (PCM) has been the subject of considerable recent interest as a potential next-generation non-volatile solid-state memory technology[1-3]. PCM has already been shown to possess many of the necessary attributes for such a technology, including high resistance contrast, a small number of new process integration steps, the potential for multi-level storage, and better endurance and write speeds than flash memory. In order to obtain the low RESET currents needed for competitive memory densities, conventional PCM approaches typically use aggressive sub-lithographic patterning of a small contact area within the memory cell.

In this paper, we demonstrate a new memory cell design, called the phase-change bridge (PCB), implemented with a promising phase-change material, GeSb. In a PCB cell, lithographic patterning has only a linear impact on the effective cross-sectional area. This offers both reduced sensitivity to variations in critical dimension, and an alternative path to rapid scaling via ultra-thin films.

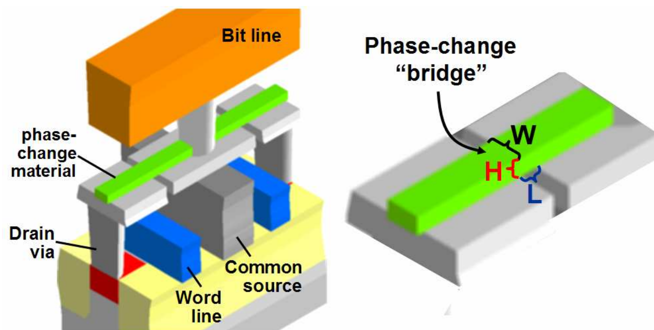

Fig. 1 Integration scheme for a phase-change bridge (PCB) memory cell. The cross-sectional area ($W \times H$) depends linearly on lithographic patterning, offering both reduced sensitivity to variations in critical dimension and an alternative path for scaling to future technology nodes via ultra-thin films.

Phase-Change Bridge Memory Cell

The phase-change bridge (PCB) device consists of a narrow line of ultra-thin phase-change material bridging two underlying electrodes. Fig. 1 shows a potential integration scheme, in which one of the two device cell electrodes connects to the drain of the underlying access transistor, while the other is connected by via up to an overlying bitline. Unlike the line-device concept published earlier as a materials test vehicle[2], here the electrodes are formed very close together to obtain a reasonable threshold voltage, separated by a small oxide gap that defines the bridge length L. The

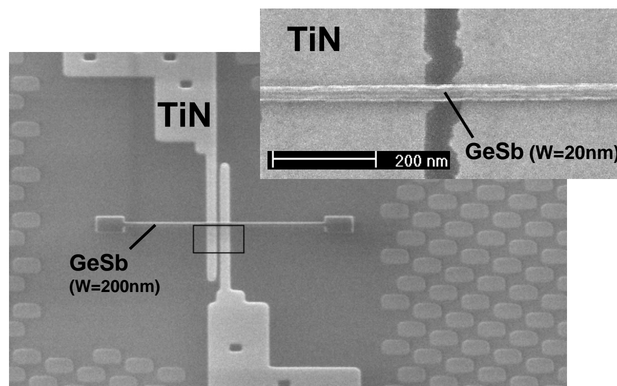

Fig. 2 SEM picture of an ultra-thin PCB memory cell test structure fabricated for proof-of-principle evaluation. Phase-change lines, patterned using e-beam in widths ranging from 20 to 200nm, bridge the TiN electrodes; the black rectangle indicates the location of the FIB cross-section in Fig. 3.

thickness of the phase-change material deposited on this planarized surface defines the bridge height H, and the width W is defined with a subsequent patterning step.

The devices tested in this work consist of bare PCB memory cells fabricated without access transistors. Starting with a thick layer of oxide on silicon, a thin spacer of photoresist was trimmed to define oxide gaps ranging from L=40 to 200nm. This was followed by etching, TiN deposition to define two parallel lead wires running to probe pads (Fig. 2), and planarization of the TiN/SiO_2 surface. An ultra-thin layer (either H=3 or 10nm) of doped GeSb was then deposited, followed immediately by 10nm of SiO_2. E-beam lithography and ion-milling were then used to define a thin line of phase-change material of width ranging from W=20-200nm (Fig. 2). The cross-sections in Fig. 3 show that an ultra-thin but robust layer of phase-change material successfully bridges the two TiN electrical contacts. The thick e-beam photoresist, shown in Fig. 3 as SiO_x, was left to protect the fragile bridge, supplemented by a 3nm blanket layer of subsequent Al_2O_3 encapsulation.

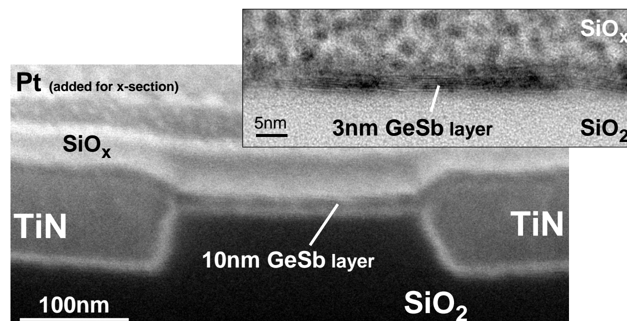

Fig. 3 This figure (inset) shows a FIB (TEM) cross-section through an ultra-thin PCB memory cell test structure with a 10nm (3nm) thick doped GeSb layer. The thick e-beam photoresist, shown as SiO_x, was left to protect the fragile bridge. Initial devices included a 3nm blanket layer of subsequent Al_2O_3 encapsulation to protect the sides of the PCB.

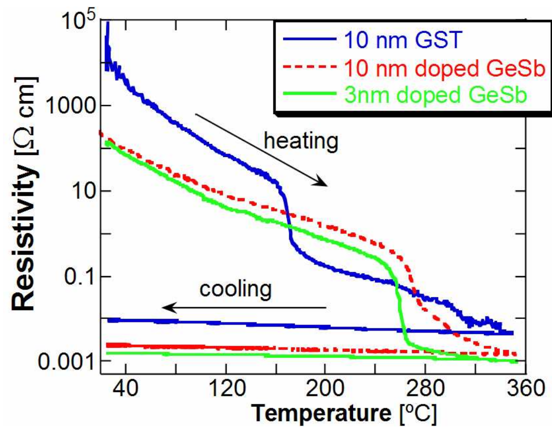

Fig. 4 Crystallization behavior from amorphous-as-deposited ultra-thin films of doped GeSb, as measured by the drop in resistivity during a slow heating ramp (1°C/sec). As compared with 10nm thick undoped $Ge_2Sb_2Te_5$ (GST), GeSb offers a significantly higher crystallization temperature.

GeSb Phase-Change Material

Fig. 4 shows the resistivity vs. temperature of doped GeSb ultra-thin films as they are crystallized at high temperature from the amorphous-as-deposited state. These doped GeSb films offer a crystallization temperature nearly 100°C higher than comparably thin films of undoped $Ge_2Sb_2Te_5$ (GST), and exhibit only moderate changes in crystallization properties even at ultra-thin film thicknesses. To evaluate the speed of doped GeSb material, a focused laser beam was used to re-crystallize amorphous spots in an otherwise crystalline film. Fig. 5 shows the resulting change in reflectivity ($\Delta R/R$) as a function of optical power and pulse duration, demonstrating fast crystallization for powers from 30–55mW. Fig. 6 focuses on this power range, showing the re-crystallization speed of doped GeSb in comparison with the best-case powers needed to crystallize undoped GST. Fig. 7 compares AFM images of partially crystallized spots in amorphous-as-deposited films. In contrast to "nucleation-dominated" GST, where crystallization is initiated from numerous locations, GeSb is a "growth-dominated" phase-change material, exhibiting very few nucleation events within each optical spot.

Figures 4–7 demonstrate that doped GeSb is a material that combines fast crystallization speed with high crystallization temperature, thus offering the potential for fast yet truly non-volatile phase-change memory.

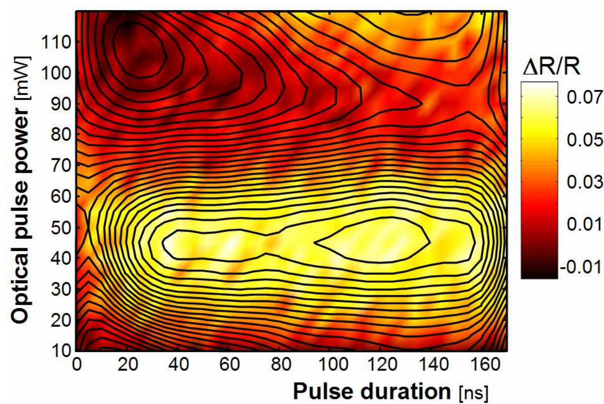

Fig. 5 Reflectivity change as a function of optical pulse power and duration for recrystallization of amorphous spots in a 20nm thick doped GeSb film (on 30nm Al_2O_3 on Si). While pulses with power >70mW result in re-melting of the phase-change material and eventually ablation, pulse powers in the range of 30-55mW produced rapid crystallization, even for pulses as short as 5nsec.

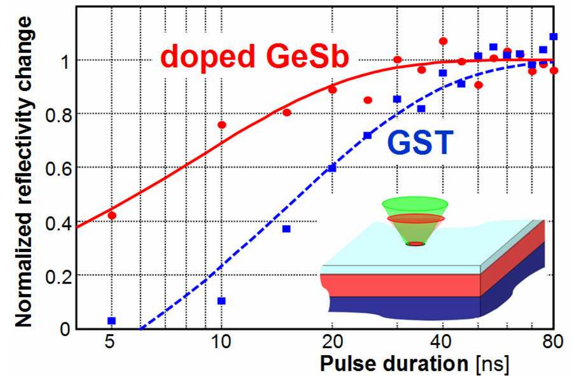

Fig. 6 Normalized reflectivity change as a function of optical pulse duration for doped GeSb as compared with undoped GST. Lines show fits to $1 - \exp(-(t - t_0)/\tau)$, with a time constant τ of 8.5nsec (15nsec) and a delay time t_0 of 0 nsec (6 nsec) for doped GeSb (GST), respectively.

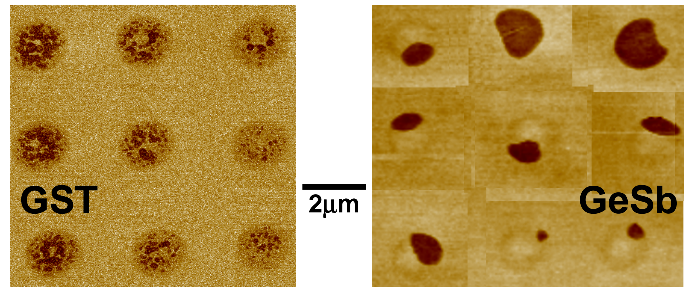

Fig. 7 AFM images of partially crystallized optical spots in otherwise amorphous-as-deposited thin films, comparing GST and GeSb via the topography change (darker color) induced during crystallization. In comparison with "nucleation-dominated" GST, where crystallization is initiated throughout the optical spot, GeSb is a "growth-dominated" phase-change material showing only a few nucleation events within each optical spot.

Electrical Characterization & Modeling

The operation of the ultra-thin PCB memory cell was modeled using a custom simulation tool, which uses finite-difference techniques to allow full 3-D modeling of arbitrary device geometries. The simulation tool solves the interaction between heat diffusion, Poisson's equation, and the phase-change process throughout the duration of a voltage/current pulse, including temperature-dependent thermal and electrical properties, latent heats of melting and crystallization, nucleation and crystal growth. Figs. 8 and 9 show the predicted 3-D distribution of phase states and temperature within the ultra-thin PCB device during a RESET step.

Electrical characterization was performed to evaluate the per-

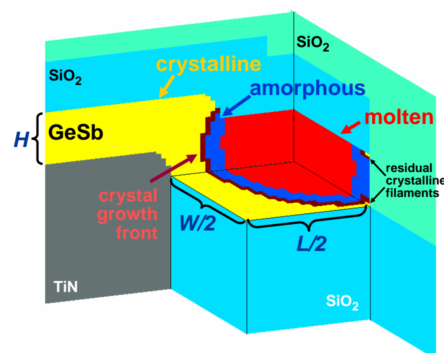

Fig. 8 Simulated 3-D distribution of phase within a PCB memory device during a RESET pulse, showing the receding melting spot as the device just begins to cool. A slightly higher pulse current would have melted the residual crystalline filaments at the device periphery, leading to a successful RESET.

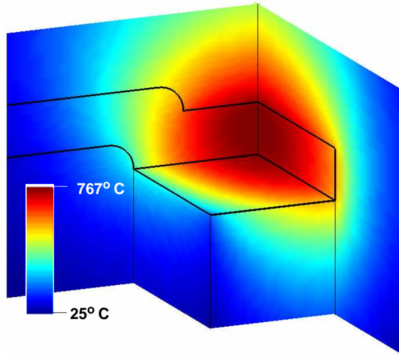

Fig. 9 Simulated 3-D temperature profile within a PCB memory device during the RESET pulse shown in Fig. 8.

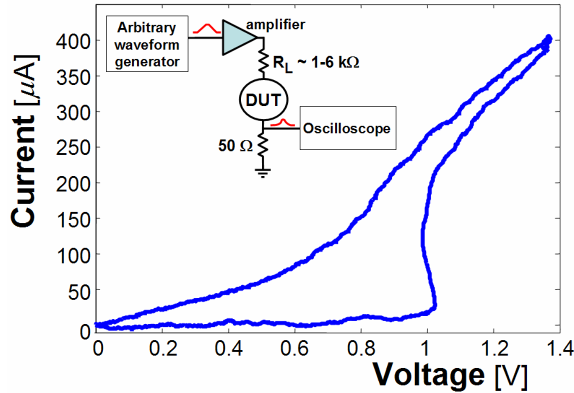

Fig. 10 IV characteristics for a PCB memory cell test structure (H=3nm, W=50nm, L=50nm), demonstrating snapback from the RESET state.

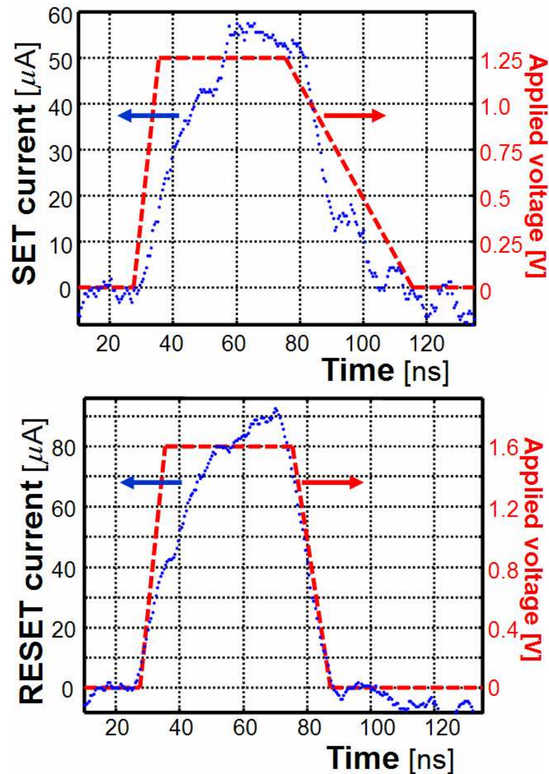

Fig. 11 Typical measured current traces for SET and RESET steps of a PCB memory cell test structure with 60nm^2 cross-sectional area (H=3nm, W=20nm, L=50nm) and minimal encapsulation, corresponding to SET (RESET) resistances of 95kΩ (500kΩ). Later devices were tested with added encapsulation, trading off an increase in RESET current (compare Figs. 11 and 12) for some improvement in lifetime.

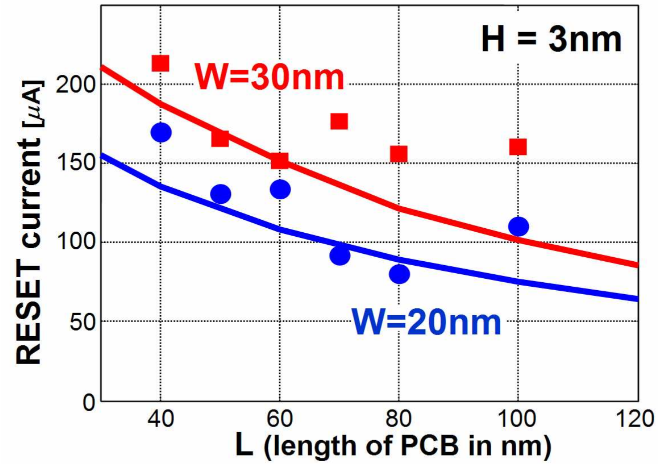

Fig. 12 Measured (symbols) and simulated (lines) RESET current of PCB memory cell test structures as a function of bridge length L, for H=3nm and W=20, 30nm. For L=70–80nm, RESET current is $<100\mu$A even with 50nm of added SiO_2 encapsulation.

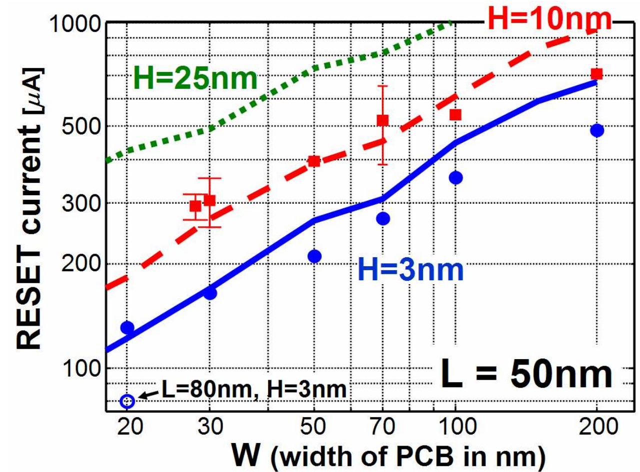

Fig. 13 Measured (symbols) and simulated (lines) RESET current of PCB memory cell test structures as a function of bridge width W, for L=50nm and H=3, 10, and 25nm (simulation only). For comparison, the open symbol shows our lowest achieved RESET current of roughly 90μA at longer bridge length L=80nm and H=3nm.

formance of the ultra-thin PCB cells. An I-V characteristic demonstrating the snapback associated with electrical breakdown of the RESET state is shown in Fig. 10. Typical measurements of RESET and SET states showed 5-20× resistance contrast, with RESET currents as low as 90μA for devices with 60nm^2 cross-sectional area (H=3nm, W=20nm, Fig. 11).

Initial device simulations were performed with the assumption that all devices of constant H would share the same resistivity; however, the experimental results did not quite follow this trend. We found that the accuracy of the simulated RESET currents were improved when the simulations were adjusted to match both the SET resistance, as well as the dynamic resistance during the RESET pulse, of each corresponding measured device. This was done by simply modeling the outer 25nm portions of the bridge width with a different resistivity than the center stripe, which suggests that the ion-milling may be modifying the doped GeSb material.

Both simulations and experiments show that RESET current is relatively constant with bridge length L, as shown in Fig. 12, with a slight improvement at larger L as the switching volume becomes more thermally insulated from the TiN electrodes. However,

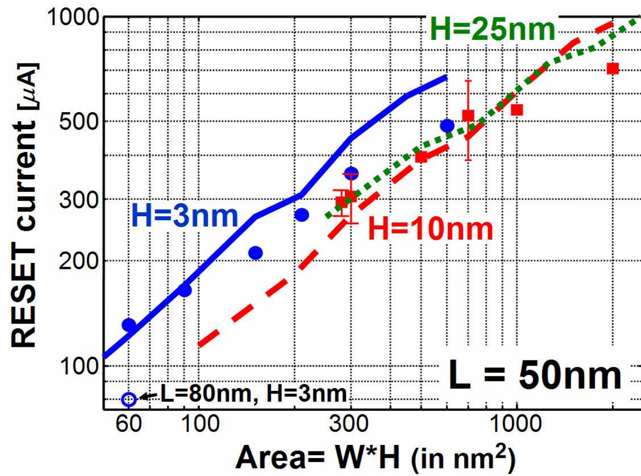

Fig. 14 Data from Fig. 13 replotted as a function of cross-sectional area $W \times H$, for L=50nm and H=3, 10, and 25nm (simulation only).

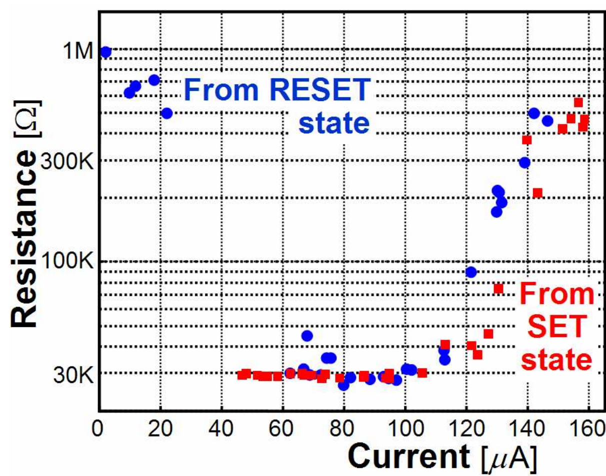

Fig. 15 R-I curve of PCB memory cell test structure (H=3nm, W=30nm, L=60nm) measured without device history, from the RESET state (circles) and from the SET state (squares). A threshold voltage of 0.8 volts, and a total SET time of 60nsec (8nsec ramp up, 40nsec plateau, 12nsec ramp down) is demonstrated.

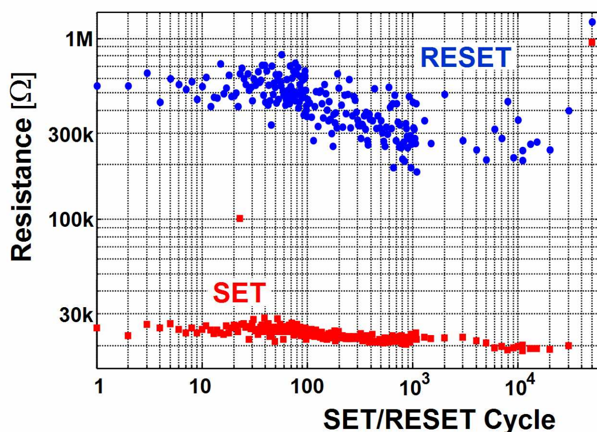

Fig. 16 Cycling data showing >30,000 SET-RESET cycles for PCB memory cell test structure (H=3nm, W=20nm, L=50nm). Avenues for further improvement of the lifetime of these ultra-thin devices, which are being switched without an integrated access transistor, might include changes in planarization, encapsulation materials, device geometry, and the electrical characterization procedures.

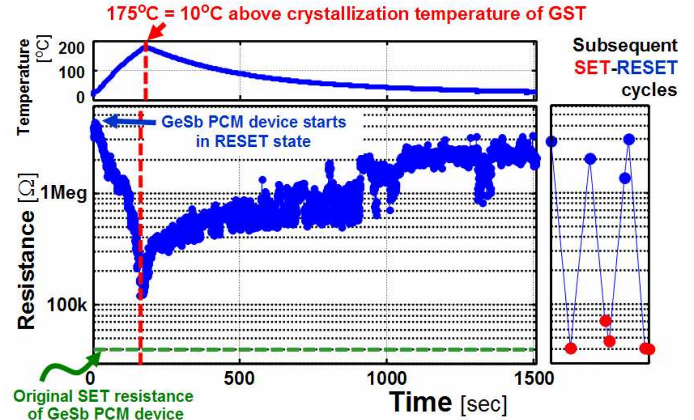

Fig. 17 Device retention test of PCB memory cell test structure (H=3nm, W=20nm, L=60nm) in the RESET state. The resistance drops with temperature as expected for doped GeSb (Fig. 4), but remains substantially above the original, room–temperature SET resistance of the device (which in turn is higher than the SET resistance to be expected at this elevated temperature from Fig. 4). Then as the device cools, the resistance returns to >1MΩ. Thus the device conclusively remains in the RESET state despite experiencing several minutes at or near ∼175°C, above the temperature at which a GST device would have already crystallized (see Fig. 4).

the RESET current drops steadily as the bridge width W gets narrower, or when thinner films are deposited to define the bridge height H (Fig. 13). As a result, the RESET current scales consistently with the cross-sectional area ($W \times H$) of the PCB device (Fig. 14). Thus the phase-change bridge device provides a unique path for scaling of cross-sectional area without excessively aggressive sub-lithographic patterning. For larger devices, a wide margin for SET and RESET could be obtained, as shown by the R-I curve in Fig. 15. While the device lifetimes observed in these tiny initial devices were sufficient to permit basic characterization (Fig. 16), we continue to explore avenues for significant improvement of device lifetime through changes in planarization, encapsulation materials, device geometry, and the characterization procedures. Encouragingly, Fig. 17 shows that data could be retained in the RESET state up to 175°C—beyond where GST would re-crystallize—showing great potential for the retention characteristics of doped GeSb.

Conclusions

The device concept, materials characterization, electrical characterization and device simulation have been shown for a novel proof-of-principle phase-change bridge memory cell implemented with doped GeSb. The device concept offers the potential for rapid scaling to small cross-sectional areas through the use of ultra-thin films, while the doped GeSb phase-change material offers the potential for both fast crystallization and good data retention at elevated temperature.

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