Electron-Beam Lithographic Studies of the Scaling of Phase-Change Memory

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Abstract

Phase-change random-access memory (PCRAM) is a promising technology for future nonvolatile storage with the added potential for possible impact on dynamic random-access memory technologies. To be successful, however, PCRAM must be able to scale to dimensions on the order of a few tens of nanometers, considering the increasingly tiny memory cells that are projected for future technology nodes. The experiments discussed in this article directly address these scaling properties, examining both the materials themselves and the operation of nanoscale devices. One series of experiments is time-resolved x-ray diffraction studies of ultrathin films and nanostructures. Electron-beam lithography was applied to pattern thin films into nanostructures with dimensions down to 20 nm. The article also includes descriptions of prototype PCRAM devices, successfully fabricated and tested down to phase-change material cross sections of 3 nm × 20 nm. The measurements provide a clear demonstration of the excellent scaling potential offered by this technology.

Introduction

Phase-change materials generally have two phases with remarkably different properties. The 30% or so change in reflectivity between phases has been exploited for many years in optical recording. However, the change in electrical resistivity is far more remarkable, reaching as much as five orders of magnitude in some materials. The basic principles of using this resistance change in a memory device have been known for over 40 years.[1] Only recently has the community recognized the potential of using these materials in crosspoint memory devices to compete with and replace existing solid-state nonvolatile devices. The renewed interest in phase-change random-access memory (PCRAM) technology was triggered by the discovery of fast-crystallizing materials such as $Ge_2Sb_2Te_5$ (GST) and Ag- and In-doped Sb_2Te.[2,3] These materials can crystallize in less than 100 ns, as opposed to the materials used for early PCRAM demonstrations such as $Te_{48}As_{30}Si_{12}Ge_{10}$, which could require 10 μs or more to crystallize.[1] These newer alloys switch more rapidly because the crystallization process generates very little atomic motion,[4] as compared to the phase segregation that occurred in the earlier, Te-rich alloys.[5]

When data are written to a PCRAM element, the phase-change material is cycled between a highly conductive crystalline state and a resistive amorphous state. The amorphous state can be crystallized by heating it to a temperature above its crystallization temperature (a so-called SET operation) and returned to the amorphous state by melt-quenching (in a RESET operation). Both SET and RESET operations are controlled by electrical current: high-power pulses place the memory cell into the high-resistance RESET state, and moderate power but longer duration pulses return the cell to the low-resistance SET state. The devices can be read by measuring resistance with very low power that does not disturb the state of the device. Figure 1 shows a typical *I–V* (current—voltage) response of a phase-change device, as well as schematic representations of typical PCRAM cells.

A critical property of phase-change materials is so-called threshold switching.[6–8] Without this effect, PCRAM would simply not be a feasible technology, because, in the high-resistance state, extremely high voltages would be required to deliver enough power to the cell to heat it above the crystallization temperature. However, when a voltage above a particular threshold is applied to a phase-change material in the amorphous phase, the resulting large electrical fields greatly increase the electrical conductivity. This effect is still not completely understood, but it is attributed to the interplay between impact ionization and carrier recombination.[6] With the previously resistive material now suddenly highly conducting, a large current flows, which can then heat the material. However, if the current pulse is switched off immediately after the threshold switching, the material returns to the highly resistive amorphous phase after about 30 ns,[9] with both the original threshold voltage and the RESET resistance recovering slowly over time.[9,10] If a current sufficient to heat the material above the crystallization temperature but below the melting point is sustained for a long enough time, the cell switches to the crystalline state (Figure 1a).

As stated, these properties make PCRAM an obvious choice for nonvolatile memory. Yet a key question remains: In order to introduce a new technology today, one would have to be convinced that it would be viable for at least a few product cycles—before committing to major investment in this technology, one would like to be confident that PCRAM will be viable at the 30-nm node in 2012 or so, and ideally beyond to the 18-nm node in 2020 or so.[11] Each technology node is associated with the smallest feature size that can be fabricated lithographically at that point in time. The question of the scalability of PCRAM technology is therefore central to its introduction and to the levels of investment.

This article begins with a review of what is known about the effect of reduced scale on phase-change properties in thin films and nanoparticles, followed by a discussion of recent studies that attempt to address the PCRAM scaling issue. Studies

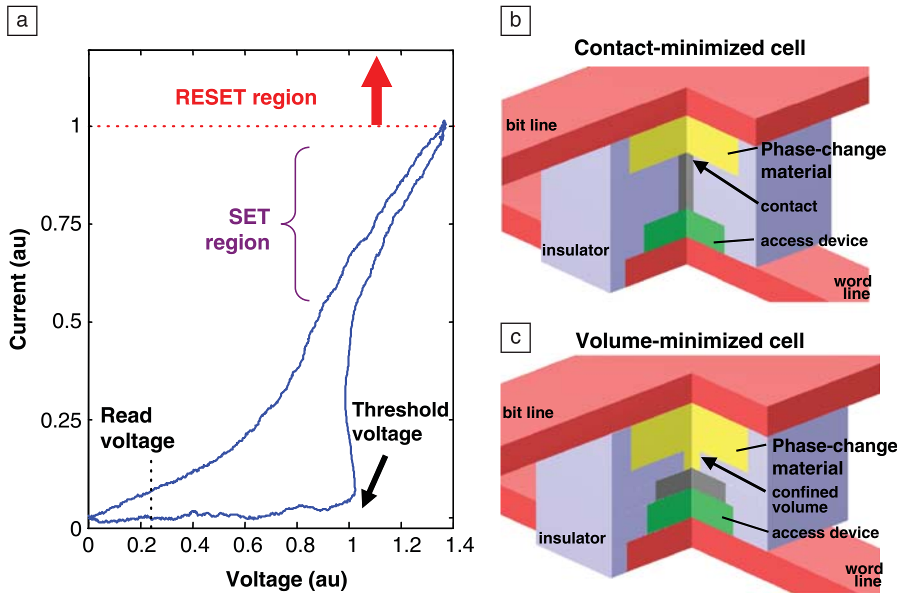

Figure 1. (a) Typical current versus voltage characteristics for a phase-change memory device, demonstrating the threshold switching and differing amounts of electrical power required for SET and RESET operations. (b) Typical phase-change "mushroom" cell, which forces current to pass through a small aperture formed by the intersection of one electrode and the phase-change material. (c) Alternative "pore" cell, which confines the volume of the phase-change material in order to create a small cross section within the phase-change random-access memory device.[47] [Reproduced with permission from Reference 47. Copyright 2006 Institute of Electrical and Electronics Engineers (IEEE).]

of the switching of phase-change materials in the form of isolated nanopillars, as well as a prototype nanobridge memory device, show recent achievements in device development. We finally conclude that, in many respects, PCRAM technology should indeed be readily scalable to several future technology nodes.

Scaling Properties of Phase-Change Materials

To predict the potential behavior of highly scaled PCRAM, it is important to determine how, and at what film thicknesses or nanoparticle dimensions, the properties of phase-change materials might be influenced by size. Important properties that can be influenced by size are the crystallization temperature and the melting point. Such scaling behavior is likely to be a function of material as well. Before considering fabricated structures, we first review previous work on the scaling properties of phase-change materials, of which dozens of variants have been developed.[12–23]

The scaling of switching properties with size has been studied by shrinking one dimension (thin films),[24–28] two dimensions (nanowires),[29–33] and three dimensions (nanoparticles)[34–42] and for a variety of phase-change materials. For thin films (shrinking of one dimension) of GST and GeSb studied with time-resolved x-ray diffraction (XRD), Raoux et al. found that the crystallization temperature (of the first crystallization from amorphous as-deposited films) increases as the film thickness is reduced.[24] Films thinner than about 20 nm showed a higher crystallization temperature than thick films and bulk material. For the thinnest films that still showed clear XRD peaks (1.3 nm thick for GeSb), crystallization occurred at about 300°C, whereas thick films crystallized at about 235°C. This increase in crystallization temperature indicates that data loss due to nucleation of new crystal nuclei within the amorphous portion of a scaled-down cell in the RESET state should actually be less likely than that in a larger cell.

For thin GST films, the amorphous–fcc phase transition also shifted to higher temperatures for films thinner than 20 nm, and increases in crystallization temperature have also been found in other PCRAM materials. For films of GST thinner than 3.6 nm, the fcc phase no longer formed. Interestingly, the hexagonal phase still formed in these very thin films of 3.6 nm and 2 nm, but no crystallization was observed in films thinner than 2 nm.[43] As demonstrated in a subsequent section, it is indeed possible to fabricate functional PCRAM cells with films as thin as 3 nm. Recording of information has also been demonstrated using 18-nm GST thin films[26] with recording densities of up to 3.3 terabits (Tb)/in.[2], by applying a nanoheater atomic force microscopy (AFM) tip. Using ultrathin GST films (1–5 nm), the smallest crystalline recording marks in an amorphous film that could be produced by an AFM tip were found to be about 10 nm.[27] Although these smallest marks disappeared within minutes, slightly larger marks (20 nm) were stable for at least 1 h. The reverse process was also demonstrated, and amorphous marks as small as about 10 nm were recorded using AFM and scanning tunneling microscopy.[25]

To further uncover the scaling behavior of materials in the form of thin films, the switching behavior of thin GST films sandwiched between layers of a composite SiO_2–ZnS material was studied by measuring the resistivity as a function of temperature.[28] It was found that the transition temperature increased as the film thickness was reduced from 100 nm to 3.5 nm. In particular, a very large increase in incubation time for crystallization was observed, for example, from about 200 ns to more than 10 µs for films of different thicknesses heated isothermally at 143.5°C. An increased activation energy correlated with increased crystallization temperature was observed.

If two dimensions are reduced in size, one obtains a nanowire. GST,[29] GeTe,[30–32] In_2Se_3,[33] and Sb_2Te[32] phase-change nanowires have been grown by the metal-catalyst-mediated vapor–liquid–solid method. These nanowires were single crystals with diameters ranging from 20 nm to 200 nm, depending on the size of the Au catalyst nanoparticles. In one case,[32] GeTe nanowires with a helical structure were formed. It was found that the melting point of GeTe nanowires was significantly reduced to 390°C compared to the bulk GeTe melting point of 725°C.[31] For In_2Se_3 nanowires, a reduction of the melting point was also observed:[33] They melted at 680°C compared to a melting point of 890°C for bulk In_2Se_3. Switching devices made of GeTe nanowires[29,30] were fabricated using the focused ion beam technique for contact formation. Pt electrodes were deposited with 2-µm separation on a nanowire. These devices showed clear threshold switching characteristics typical for phase-change devices and could repeatedly be switched between the amorphous and crystalline phases using an electrical current pulse.

If all three dimensions are reduced, one obtains nanoparticles. Phase-change nanoparticles have been fabricated and studied using a variety of methods.

Fabrication methods have included pulsed laser ablation, electron-beam lithography, and lithography based on the self-assembly of polymers. Pulsed laser ablation is a relatively easy and inexpensive method for nanoparticle fabrication; the particles can be very small, but the size distribution is typically not very narrow. Electron-beam lithography results in very precise particle size and location (see next section), but it is time-consuming and expensive, and the particle size is limited by the resolution of the lithography. Self-assembly-based techniques can fabricate smaller particles than electron-beam lithography (see also next section) with relatively narrow size and distance distributions but no precise location control.

Pulsed laser ablation was used to fabricate GST nanoparticles with sizes between 5 nm and 50 nm.[34,36,37] PCRAM devices were fabricated using multiple layers of GST nanoparticles produced by laser ablation,[34] and both threshold switching and repeated cycling of the devices were demonstrated. Yoon et al.[37] reported that, for particles exposed to temperatures of 100°C, 200°C, 300°C, and 400°C, in all cases, the particles had crystalline regions in the fcc phase. They also observed other crystalline phases, presumably due to off-stoichiometric Ge–Sb–Te regions. Choi et al.[36] observed that crystallization of the nanoparticles occurred for temperatures between 200°C and 300°C and that nanoparticles crystallized at these temperatures showed both the fcc and hexagonal phases whereas nanoparticles heated to temperatures higher than 400°C showed only the fcc phase. This result is surprising because, in thick films and bulk GST, it is known that the fcc phase is the metastable phase, appearing at about 150°C and being transformed into the stable hexagonal phase at around 350–400°C.[44]

Phase-Change Studies of Nanoparticle Arrays

To address the issue of phase-change scaling more directly, the switching of fabricated arrays of near-identical encapsulated phase-change nanoparticles was examined. By fabricating the nanoparticles using techniques similar to those used for device fabrication, results can be obtained that are even more relevant to the issue of scaling in devices. Thus, the crystallization behavior of large arrays of phase-change nanoparticles of various materials fabricated by electron-beam lithography was studied in one investigation and the associated phase transitions were examined using time-resolved XRD.[41] Specifically, nanoparticles fabricated from $Ge_2Sb_2Te_5$ and $Ge_{15}Sb_{85}$,[24,42] as well as $Ge_2Sb_2Te_5$, nitrogen-doped $Ge_2Sb_2Te_5$, $Ge_{15}Sb_{85}$, Sb_2Te, and Ag- and In-doped Sb_2Te, were studied.[41] These materials were selected because of their relevance for applications. PCRAM devices have been described in the literature that employ these materials, and several of these materials are also used in rewritable CDs and DVDs.

Thin films of the phase-change materials were deposited by sputter deposition on to SiO_2-coated Si wafers. The films were 50 nm thick. The GST, Sb_2Te, and Ag- and In-doped Sb_2Te were sputtered from nominally stoichiometric targets, and the actual film compositions were Ge(23%) Sb(29%)Te(48%), Sb(74%)Te(26%), and Ag(8%) In(10%)Sb(50%)Te(32%). The nitrogen-doped GST was deposited and had a film composition of N(2%)Ge(23%)Sb(28%)Te(47%).

Nanostructures of these materials were fabricated by electron-beam lithography. There were two major challenges in this work: the fragile nature of the materials and the large (2 mm × 5 mm) patterned areas required for the XRD studies. A lithographic process had to be selected that would not lead to damage of the phase-change material (as, for example, reactive-ion etching is known to cause) and that did not require temperatures that would crystallize the nanoparticles. The films were spin coated with ~100 nm of poly(methyl methacrylate) (PMMA) resist and heated at only 110°C, which is low enough to avoid the phase transition temperatures, which are between 120°C and 250°C. After the samples had been patterned and developed, Cr was deposited by evaporation. A hot solvent removed the resist, leaving Cr dots on the film surface. The dots acted as a hard mask protecting the film during ion milling. The mass peaks of the phase-change materials during milling were monitored using secondary ion mass spectroscopy. The mill time was calculated to be sufficient to remove over 12 nm of Cr, so it is expected that only a few nanometers of Cr cap were left. The samples were then encapsulated in 10 nm of alumina. It has been shown previously that a 10-nm alumina capping layer is very efficient in preventing oxidation of phase-change materials.[24]

Using this basic approach, nanopatterned arrays with pillar diameters in the range between 80 nm and 20 nm were fabricated. Although the pitch was 80 nm in some cases (for the smallest patterns), in most cases, the pitch was 100 nm. The 2 mm × 5 mm area of the nanopatterned arrays was larger than the area of the x-ray beam used to study the crystallization behavior. Great care was taken in the fabrication process to keep the temperatures below the crystallization temperature of the respective material. Figure 2 shows a high-resolution transmission electron microscopy image of a $Ge_{15}Sb_{85}$ nanoparticle after it has been heated in a purified He atmosphere to 450°C. It is evidence that the small volume can crystallize, showing polycrystalline grains about 10 nm in size. The 10-nm-thick Al_2O_3 encapsulation layer is clearly visible in Figure 2.

The crystallization behavior of the arrays was studied using time-resolved XRD, which revealed that all nanoparticle arrays with particle sizes between 20 nm and 80 nm exhibited clear evidence of crystallization at temperatures similar to those of thick films of the same material. Figure 3 shows XRD peak intensities as a function of temperature for a GeSb blanket film compared to those of nanostructures.[24] Both films and nanostructures were heated to 430°C at 1°C/s. It can be seen that there is little difference in the temperature of the phase transition, which remains near 230°C. In fact, there is a small decrease in the phase transition temperature with decreasing size, as summarized in Figure 4.[24] One exception to this general behavior was found for Sb_2Te, which showed an increased crystallization temperature (40°C higher) compared to thick films. In addition, GST phase-change nanoparticles were found to show only the fcc phase for the smallest particles (20 nm), whereas larger particles exhibited a behavior similar to that of thick films and bulk material.[41] GST thin films seem to behave differently from GST nanoparti-

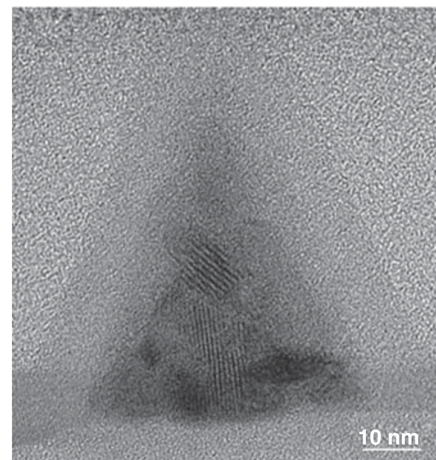

Figure 2. High-resolution bright-field transmission electron microscopy image of an annealed GeSb nanoparticle.[41] The figure shows that a volume as small as this nanoparticle still can clearly crystallize. (Reproduced with permission from Reference 41. Copyright 2007 American Institute of Physics.)

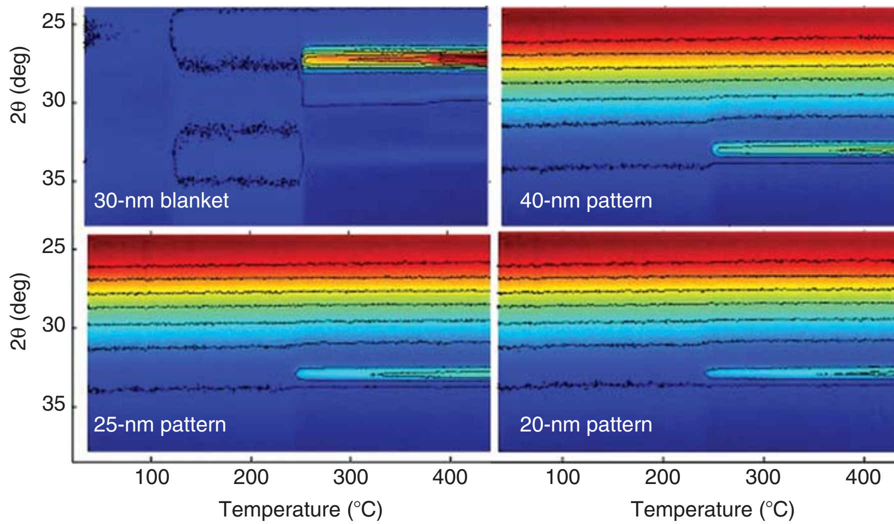

Figure 3. Intensity of diffracted x-ray peaks as a function of temperature during the 1°C/s heating of (a) a 30-nm-thick GeSb blanket film and GeSb nanopatterned samples composed of (b) 40-nm, (c) 25-nm, and (d) 20-nm nanoparticles.[24] As-deposited films and as-fabricated nanoparticles are amorphous, and there is no significant x-ray diffraction. When the samples are heated and reach their crystallization temperature, suddenly diffracted x-rays can be detected. The diffraction angle 2θ depends on the crystal structure of the materials and the x-ray wavelength used. (Reprinted with permission from Reference 24. Copyright 2006 EPCOS.)

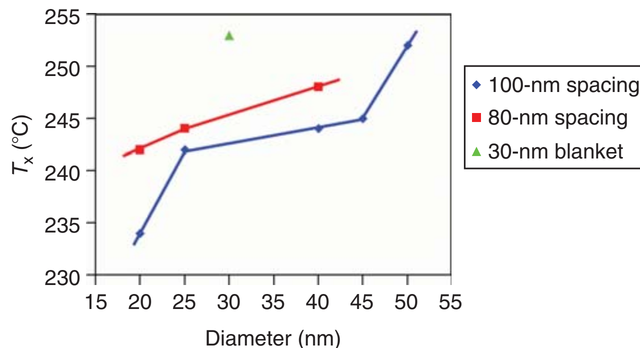

Figure 4. Crystallization temperature (T_x) as a function of pattern size for GeSb nanostructures. (Reprinted with permission from Reference 24. Copyright 2006 EPCOS.)

cles, with the thinnest films forming only the hexagonal phase and not the fcc phase.

To further reduce particle size beyond the limit of electron-beam lithography, self-assembly-based lithographic techniques were applied to fabricate phase-change nanoparticles.[38–40] Self-assembled PS-*b*-P4VP [polystyrene-*b*-poly(4-vinylpyridine)] on top of an amorphous GeSb phase-change film was used to locally grow SiO_2 dots on top of the P4VP domains.[38,39] Reactive-ion etching and ion milling were then applied to transfer the pattern into the GeSb using the SiO_2 dots as a hard mask. Time-resolved XRD performed on the nanoparticle arrays demonstrated that these 15-nm-diameter particles clearly crystallized at a temperature that was 15°C lower than that of comparable blanket film. In another experiment, PS-*b*-PMMA [polystyrene-*b*-poly(methyl methacrylate)] films were used, with phase-change nanoparticles fabricated by PMMA removal, deposition into the PS-*b*-PMMA template, and liftoff.[40] AIST nanoparticles of about 20-nm diameter were obtained that showed a crystallization temperature of 175°C, slightly higher than that of a blanket film (165°C).

Scaling Demonstrator: The Phase-Change Bridge

Although studies of the scaling properties of phase-change materials and pillars can provide a proof of the concept that the materials are at least capable of undergoing transitions when confined to small dimensions, the ultimate verification of scaling requires the building of actual prototype devices. Moreover, such prototype devices can provide additional vital information on the scaling of PCRAM device properties. Although simulations and analysis have long predicted that the RESET current should be reduced when the device dimensions are reduced,[45] the exact value and slope of this reduction depend significantly on simulation parameters, which are not always well known. Thus, the fabrication of devices that vary in size is critical for the quantitative calibration and verification of such models. In addition, experimental demonstration of prototype devices provides tangible proof that ultrascaled phase-change memory devices do indeed work. A number of factors can be evaluated that are not easily simulated, such as changes either in the degradation mechanisms or in the phase-change dynamics in the presence of increased surface and interface effects.

Several groups have studied phase-change memory scaling.[12,46] By measuring the RESET current experimentally, Pirovano et al. showed that, even when the contact area between the phase-change materials and the electrode is only ~300 nm^2, the devices still function properly.[46] Lankhorst et al. described a phase-change line device with cross-sectional areas as small as 225 nm^2 that could be switched repeatedly.[12] However, if one assumes that the sublithographic size of the phase-change critical dimension will be equal to 30% of the smallest achievable lithographic dimension,[11] then these 15-nm phase-change critical dimensions roughly correspond to the 45-nm lithography node. This technology node will likely be in use by the flash memory industry as soon as the year 2009.[11] To see how PCRAM might operate further along this roadmap, it is of great interest to try to scale the device cross section further still.

A device designed to study scaling in actual devices, called the phase-change bridge (PCB) and shown in Figure 5a, consists of a narrow line of ultrathin phase-change material bridging two underlying electrodes.[47] Unlike in earlier line-device concepts,[12] here the electrodes are formed very close together to obtain a reasonable threshold voltage, separated by a small oxide gap that defines the bridge length L. The cross-sectional area ($W \times H$) depends linearly on lithographic patterning, offering both reduced sensitivity to variations in the critical lithographic dimension and an alternative path for scaling to future technology nodes through ultrathin films.

The process flow of the device is shown in Figure 6, together with representative

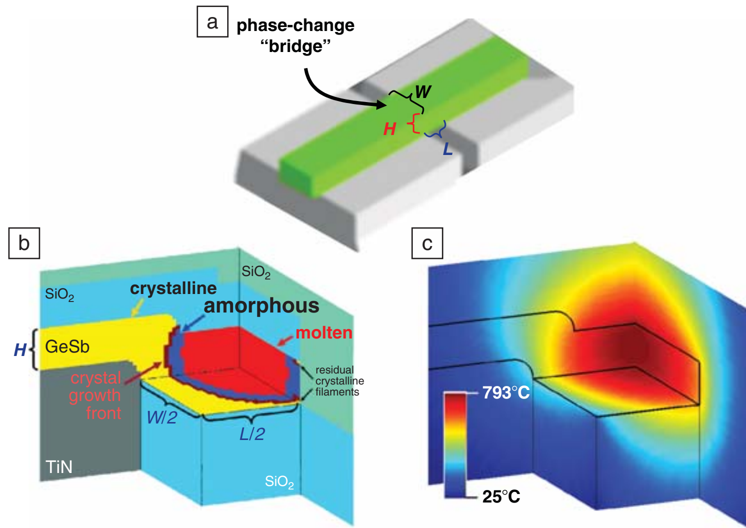

Figure 5. (a) In the phase-change bridge (PCB) memory cell, the cross-sectional area ($W \times H$) has only one dimension that depends on lithographic patterning, making it possible to greatly reduce the second dimension through ultrathin films. Simulated three-dimensional distributions of (b) phase and (c) temperature within a PCB memory device during a RESET pulse, showing the receding melting spot as the device just begins to cool. A slightly higher pulse current would have melted the residual crystalline filaments at the device periphery, leading to a successful RESET.[47] (Reproduced with permission from Reference 47. Copyright 2006 IEEE.)

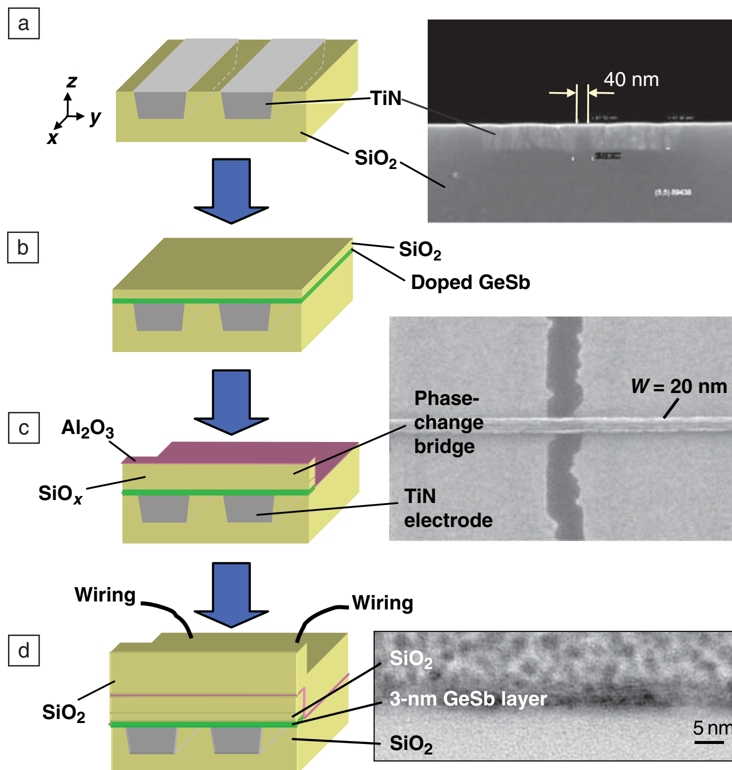

Figure 6. Schematic illustrations of the steps used in fabricating the bridge device. (a) Three-dimensional drawing and cross-sectional scanning electron microscopy image after TiN electrode fabrication. (b) Three-dimensional drawing after SiO_2 deposition. (c) Three-dimensional drawing and a plain-view scanning electron microscopy image after Al_2O_3 encapsulation. (d) Schematic plot and cross-sectional transmission electron microscopy image after full fabrication.[47] (Reproduced with permission from Reference 47. Copyright 2006 IEEE.)

scanning electron microscopy and transmission electron microscopy images. First, conventional 248-nm KrF lithography and etching was used to fabricate two parallel trenches in SiO_2 separated by a very narrow SiO_2 layer (from 40 nm to 1,000 nm). After the trenches had been filled with thick Ti/TiN by sputter deposition and the samples had been subjected to chemical–mechanical polishing, wafers were obtained with two TiN electrodes separated by a small SiO_2 gap (Figure 6a). A doped GeSb phase-change material with thicknesses between 3 nm and 10 nm was then deposited using magnetron sputtering, followed immediately by a 10-nm SiO_2 cap layer to prevent oxidation of the phase-change material (Figure 6b). Electron-beam lithography was then used to form the bridge structures with widths between 20 nm and 200 nm. After the final ion milling step, another cap layer of 5 nm of Al_2O_3 was deposited onto the device without breaking vacuum in order to prevent oxidation (Figure 6c). Note that the hydrogen silsesquioxane resist used to define the device does not need to be removed; the remaining resist forms part of the capping structure. To further protect the whole device, a thick capping layer (50 nm of SiO_2) was deposited before the device was wired for testing (Figure 4d).

These phase-change bridge devices were electrically tested using a custom setup designed for prototype PCRAM devices.[48] An arbitrary waveform generator was used to produce current pulses with rise and fall times shorter than 2.5 ns. Such pulses are required because the doped GeSb material shows very fast recrystallization, as fast as 10–20 ns in optical characterization experiments.[47] The current–voltage characteristics of these devices exhibited both threshold switching and proper device performance (switching between SET and RESET states), even down to the smallest cross-sectional areas of 60 nm² (H = 3 nm, W = 20 nm). This rectangular cross-sectional area corresponds to a cylindrical phase-change critical dimension of 9 nm, commensurate with a minimum lithographic feature size of 30 nm. Thus, these PCB devices provide strong experimental evidence that PCRAM devices could potentially scale at least through the 32-nm device generation, which the flash memory industry is expected to reach in the year 2013.[11]

SET pulses as short as 40 ns could be used to switch the phase-change bridge without sacrificing the ratio between the RESET and SET state resistances. Because such speeds are not easily obtained even in large GST-based devices, these results are

due to the inherently fast switching found in the doped GeSb phase-change material. Optical testing of a blanket film of this material[47] also showed significant speed improvements over GST. Thus, this doped GeSb material offers a unique combination of fast switching, a very high difference in resistivity between the amorphous and crystalline phases (more than four orders of magnitude), high crystallization temperatures, and the capability of operating even down to phase-change material thicknesses of 3 nm.

As predicted by simulations, the RESET current scales directly with the cross-sectional area of the device. Simulations show that the RESET condition is dictated not by the maximum temperature at the cell center, but by what happens at the edge of the cell. For instance, as shown in Figure 5b, a voltage pulse just below the RESET condition invariably resulted in some small portion of the limiting cross-sectional aperture remaining in the crystalline state, usually at the extreme edges of the cell.[47]

A comparison of experimental results with simulations for the RESET current is shown in Figure 7. For the smallest devices fabricated in this study, with a cross section of 20 nm × 3 nm, the RESET current was as low as ~80 μA. As predicted, the lowest RESET current was not obtained with the shortest device lengths.[47] This effect is due to a balance between the excessive heat loss to the metal electrodes that occurs at short lengths and the poor power efficiency that comes from distributed heating of a long phase-change bridge.

With careful design of the surrounding material and structure, the RESET current can potentially be further reduced. For instance, modifying the process just described, it was possible to fabricate phase-change bridge devices with 5-nm-thick TaN electrodes (instead of 80-nm-thick TiN). This allowed the RESET current to be reduced by roughly 40% (Figure 7).[47]

Typically, phase-change bridge devices could be cycled through more than 10,000 SET–RESET cycles. Thermal retention was tested by measuring the resistance of a phase-change bridge device programmed into the RESET state while it was being

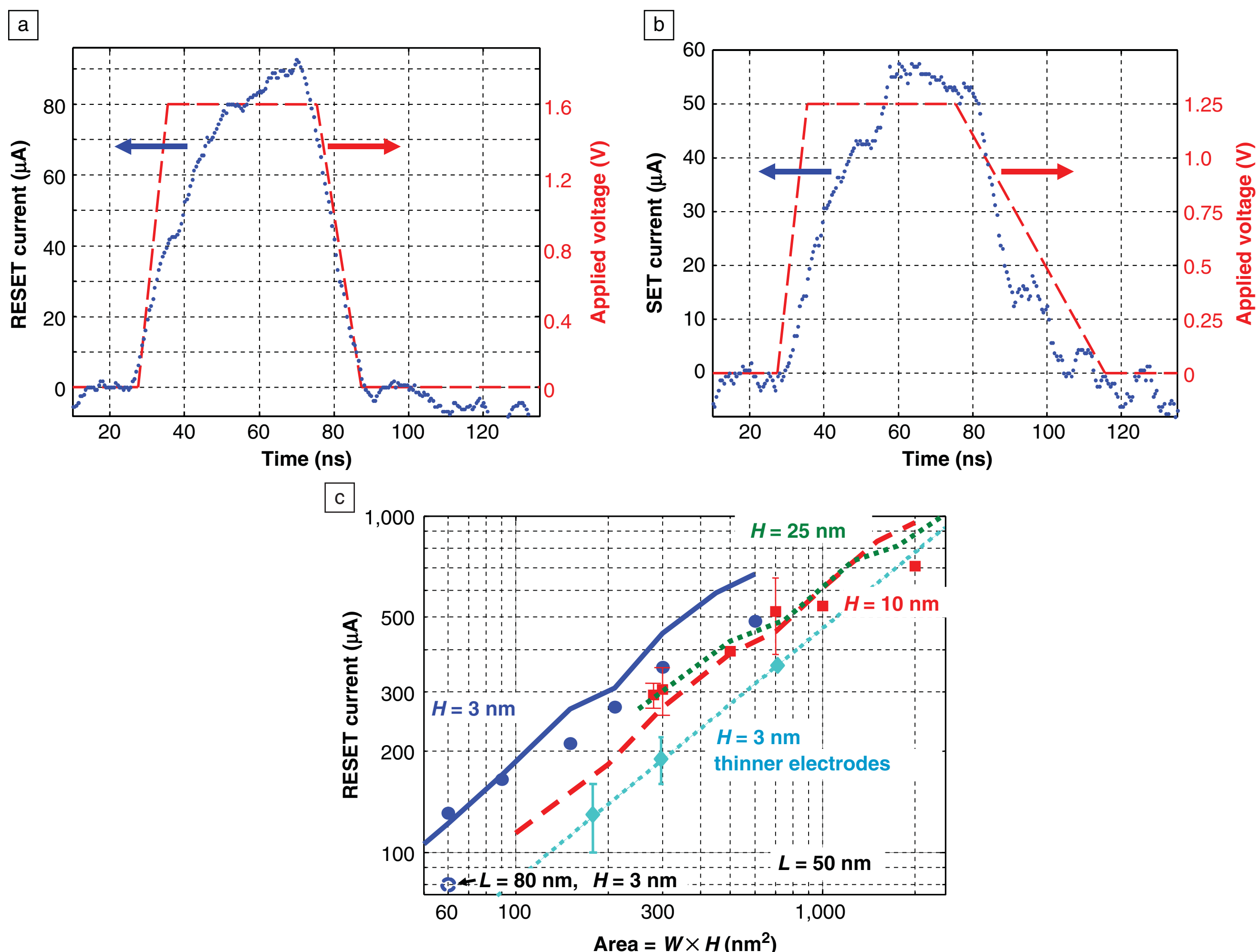

Figure 7. Typical measured current traces for (a) RESET and (b) SET steps of a prototype phase-change bridge memory cell with 60-nm² cross-sectional area (H = 3 nm, W = 20 nm, L = 50 nm) and minimal encapsulation, corresponding to a RESET (SET) resistance of 500 kΩ (95 kΩ). (c) Measured (symbols) and simulated (lines) RESET current of prototype phase-change bridge memory cells as a function of bridge width W, for L = 50 nm and H = 3, 10, and 25 nm. For comparison, the open symbol shows our lowest achieved RESET current (with 80-nm-thick TiN electrodes) of roughly 80 μA. The light blue diamonds, along with a fit through the data to guide the eye, show the reductions in RESET current made possible by reducing the heat loss through the electrodes, which, in turn, was made possible by reducing the electrode thickness and changing from TiN to TaN.[47] (Reproduced with permission from Reference 47. Copyright 2006 IEEE.)

heated. As expected from the measured dependence of resistivity on temperature in doped GeSb, the device resistance decreased as the temperature increased. After being heated to 175°C at a rate of 1°C/s, the device was cooled and found to have returned to a high-resistivity state. A device fabricated from GST would have fully crystallized at these temperatures, losing the stored data. However, the final resistance in the doped GeSb device was approximately only 50% of the value of the initial resistance, so only a modest amount of recrystallization had taken place. The advantage of doped GeSb is to push the point at which data loss occurs to higher temperatures.

Conclusions

In this article, we analyzed the scaling behavior of PCRAM technology in terms of the scaling properties of the phase-change materials themselves and the performance of actual ultrascaled prototype devices. We showed that the properties of phase-change materials are generally conserved down to dimensions of just a few nanometers, and we described functioning devices made using films as thin as 3 nm, with cross-sectional areas of only 60 nm^2. We conclude that PCRAM technology should be readily scalable to several future technology nodes.

Acknowledgments

There are many people we need to acknowledge, all of whom helped in some way with this work. The experimental device work described here was performed as part of the IBM Qimonda Macronix PCRAM Joint Project, involving, in addition to the present authors, M.J. Breitwisch, R.M. Shelby, S.-H. Chen, H.-L. Lung, C.H. Lam, T. Nirschl, T.D. Happ, E. Joseph, A. Schrott, C.F. Chen, J.B. Philipp, R. Cheek, M.-H. Lee, W.P. Risk, G.M. McClelland, Y. Zhu, B. Yee, M. Lamorey, B. Rajendran, S. Zaidi, C.H. Ho, P. Flaitz, J. Bruley, R. Dasaka, S. Rossnagel, M. Yang, and R. Bergmann. We also gratefully acknowledge our collaborators D. Milliron, M. Salinga, D. Krebs, and J. Jordan-Sweet, as well as processing support from the Microelectronic Research Line at Yorktown Heights; expert analytical and other support from the Almaden Research Center (V. Deline, T. Topuria, A. Kellock, P. Rice, D. Miller, C.M. Jefferson, J. Cha, Y. Zhang, M. Caldwell, P. Green, and K. Appavoo); physical failure analysis (M. Hudson, L. Garrison, M. Erickson); and valuable discussions with M. Wuttig, B. Kurdi, C. Narayan, K. Gopalakrishnan, R. Shenoy, W. Gallagher, R. Liu, G. Mueller, and T.C. Chen.

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