Endurance and Scaling Trends of Novel Access-Devices for Multi-Layer Crosspoint-Memory based on Mixed-Ionic-Electronic-Conduction (MIEC) Materials


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Abstract
We demonstrate compact integrated arrays of BEOL-friendly novel access devices (AD) based on Cu-containing MIEC materials[1-3]. In addition to the high current densities and large ON/OFF ratios needed for Phase Change Memory (PCM), scaled-down ADs also exhibit larger voltage margin $V_m$, ultra-low leakage (<10pA), and much higher endurance (>10^8) at high current densities. Using CMP, all–good 5 × 10 AD arrays with $V_m > 1.1$V are demonstrated in a simplified CMOS-compatible diode-in–via (DIV) process.

Keywords: Access device, MIEC, PCM, NVM, MRAM, RRAM

Introduction
For PCM or any other nonvolatile memory (NVM) to be as cost-effective as NAND FLASH (≤ $4F^2$/3), 3D-stacking of large crosspoint arrays in the BEOL is essential[4-5]. MIEC materials offer the requisite high ON current densities, low OFF current, and <400° processing temperatures[1]. However, large arrays mandate a wide voltage margin (to avoid excessive leakage through both half- and un-selected devices), and the AD characteristics must not degrade during memory operation, even as PCM current densities steadily increase with scaling (Fig.1)[1,6].

MIEC device fabrication and characteristics
In the first of three prototype AD designs that have been fabricated (Fig.2(a)), our Cu-containing MIEC material and a non-ionizable, wide-area TEC (≡ BEC) are sputter-deposited into an e-beam-defined via. In the second (Fig.2(b)), the TEC is patterned with e-beam and ion-milling, which enables bipolar operation (in-set). For both wide-area- and confined-TEC ADs, a polysilicon resistor allows current measurement during high-speed pulsing. Fig.3 shows cycling of a PCM pore device through an overlying confined–TEC AD. The 33nm pore-cell PCM, not just near the TEC. Such device arrays, tested using the integrated FETs, repeatedly exhibit 100% yield (Fig.5), with tightly-distributed voltages corresponding to PCM programming at sub-45 nm technologies, as the number of displaced ions drops. Encouragingly, arrays of DIV ADs damaged by excessive cycling can be recovered with a simple thermal anneal (Fig.12(a)); initial results with single DIV ADs, partially degraded by high-currents of one polarity, show similar recovery upon brief exposure to high current in the opposite direction (Fig.12(b)).

Scaling, new materials and voltage margin
Voltage margin $V_m$ must be high to enable large arrays of cross-point memory devices[1]. Fig. 13 reaffirms[1] that as MIEC-based ADs are scaled in TEC area (and thus in MIEC volume), the $V_m$ of confined ADs increases markedly. DIV access devices fabricated with CMP show even higher voltage margins (1.1V), and extend a universal trend of $V_m$ with TEC CD (Fig.13). This strong dependence, together with Conductive-AFM (C-AFM) observations on MIEC thin films that $V_m$ is independent of thickness down to 20 nm, indicates that the AD scaling called for by Fig.1 will inherently improve $V_m$. New materials have also been explored with C-AFM to further improve the voltage margins (Fig.14).

Conclusions
We have demonstrated compact integrated arrays of BEOL-friendly novel access devices (AD) based on MIEC materials. Significant improvement in the endurance was achieved through reductions in film thicknesses and currents. Endurance was also shown to be CD-independent, leading to > $10^9$ cycles of endurance for currents corresponding to PCM programming at sub-45 nm technology nodes. Using a simple 1-mask BEOL-compatible CMP process, all-good 5 × 10 AD arrays with $V_m > 1.1$V and ultra-low leakages were demonstrated. Sizeable further $V_m$ improvements are anticipated from device scaling and new materials.

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References
Fig. 1 PCM requires large Access Device (AD) current densities, yet absolute RESET current will decrease with scaling.

Fig. 2 MIEC-based ADs with non-ionizable electrodes are fabricated on 4” wafers with a) wide-area TECs (> BEC), b) TECs patterned to enable bipolar operation (inset) with ion-milling, and c) on 8” wafers with integrated FETs using Chemical-Mechanical Polishing (CMP).

Fig. 3 Cycling of a 33nm pore-cell PCM, with SET, RESET, and read performed through an overlaying AD (80nm BEC), which showed no degradation despite the >10⁷ high-current pulses. The 200nm TEC allowed “good polarity” (positive-on-TEC) PCM operation[7].

Fig. 4 a) Top-down view of metal- and MIEC-vias for a 5x10 array (w/ dummy rows/columns), after CMP; (b) TEM cross-section of a Diode-In-Via (DIV) AD, with planarized MIEC material capped by the TEC.

Fig. 5 Measured i-v characteristics for a 5x10 array of DIV ADs, tested with integrated FETs, showing large voltage margin (V_{tm} ~ 1.1V) and tight distributions.

Fig. 6 Slow measurements, performed on single or multiple good devices, reveal that leakage currents in MIEC-based ADs near 0V are <10nA.

Fig. 7 Both a) wide-area TEC and b) DIV MIEC-based ADs can operate without degradation for many high-current pulses, but eventually a change from low- to high-leakage occurs. This change is abrupt in all but the thickest ADs.

Fig. 8 MIEC-based AD endurance depends on current, but is independent of BEC CD, despite the nearly 3-fold change in current density.

Fig. 9 ADs show better endurance as the thickness, and thus the volume from which Cu⁺ is accumulated during cycling (see Fig.11), becomes smaller.

Fig. 10 For both wide-area TEC and DIV ADs, endurance improves as pulse duration is reduced.

Fig. 11 Local stoichiometry from TEM/EELS of wide-area TEC, 80nm BEC ADs a) as-fabricated, and b) after 425,000 cycles at 325μA. Regions near the TEC (biased negative for cycling) have become markedly Cu-rich.

Fig. 12 Low-leakage i-v characteristics that have been degraded by endurance failure or high-current pulses can be recovered by either a) thermal annealing, or b) high-current pulses of the opposite polarity. This implies that local accumulations of Cu shown in Fig.11 can be successfully redistributed.

Fig. 13 Wide-area-TEC, confined-TEC, and DIV ADs exhibit a common trend: V_{tm} increases sharpy as TEC CD is scaled down.